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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,565	02/22/2002	Eliezer Pasternak	2100259-991141	1996

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,565	PASTERNAK ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *23-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 31-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on March 10, 2003. These drawings are not approved.

The modified figure 2 is not clear. Insulation layer 10 and metal shield layer both are shown with the same cross section. Further, in the modified figure 2, the metal coating layer on the insulation layer of the wire 9 is not shown.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uematsu et al., US Patent 5,847,453, hereafter Uematsu, in view of Yoshida et al., US Patent 6,590,479, hereafter Yoshida.

Regarding claim 1, Uematsu discloses an electrical component package comprising:

a base to accommodate one or more electrical components on its surface (base plate 3, see figure 3, column 3, line 25-30), and

one or more coaxial vias formed in base for input / output of electrical signals from the electrical component (terminals 34-37 and insulators 34a-37a), but

fails to disclose each of the coaxial vias and the base form a substantially flat surface.

Yoshida discloses a metal substrate 12 with vias having central core 15 with a ring of insulator material 14, see figure 1A, column 3, line 55 to column 4 and line 5 and further discloses a coplanar transmission lines, figure 5B, column 7, line 10-15 coplanar transmission lines.

A person of ordinary skill in the art would use either of the substrate of Yoshida, either to figure 1A or 5B, depending upon the specific connection requirement for the desired functionality.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Uematsu with coaxial vias and the base form a substantially flat surface, as taught by Yoshida, in order to have the connections of the component for the desired functionality.

Regarding claim 2, the combination of Uematsu and Yoshida further discloses the coaxial via comprises a central conductive contact area surrounded by an insulating material ring, see figure 1 of Uematsu and figure 1A and 5B of Yoshida.

Regarding claim 8 and 9, the combination of Uematsu and Yoshida further discloses metallic base plate, which will inherently be electrically and thermally conductive (Uematsu, metallic base plate 3, column 3, line 39-45).

Regarding claims 10, though the combination of Uematsu and Yoshida does not explicitly disclose the thermal expansion coefficient of the component and the base, it is conventional in the art to match or adjust the thermal expansion coefficient of the substrate to that of the component in order to avoid the damage or breakage of the connection structure.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of the combination of Uematsu and Yoshida with the base material with the thermal expansion coefficient matched to that of the component, in order to avoid the damage to connection structure or the component.

Regarding claims 11 and 12, the applicant is claiming a solder mask on the coaxial via and on the surface on the package edge. Though the combination of Uematsu and Yoshida does not disclose such mask, providing solder mask is known in the art to avoid spreading of the solder at the connection point causing short circuit. Further, the mask will protect the circuit surface from damage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of the combination of Uematsu and Yoshida with the solder mask in order to avoid any short-circuiting.

4. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Uematsu and Yoshida as applied to claims 1-2, and 8-12 above, and further in view of Japanese Patent No. JP2001015654A, hereafter JP654.

Regarding claim 33, as understood by the examiner, the combination of Uematsu and Yoshida does not disclose a conductive layer having second diameter connected to central conductive area.

JP654 discloses connecting terminal 6 and 7 on the central conductive area.

Such conductive layers are known in the art for better connection of the component lead to the via terminal and this design will help in reducing the size of the pad above the via hole to increase the via density and further the size will be decided based on he component lead size.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of the combination of Uematsu and Yoshida with a conductive layer having a second diameter on the central conductive contact are, as taught by JP654, in order to have the pad of desired size to have better electrical and mechanical connection of the component element to the pad.

Regarding claim 34, the combination of Uematsu and Yoshida and JP654 further discloses a conductive layer electrically connected to the central conductive contact area and a part of the insulating material ring that is adjacent to the central conductive area, see JP654, figure 1.

5. Claims 3-4, 13-15, 19-22, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Uematsu and Yoshida, as applied to claims 1-2, and 8-12 above, and further in view of Zechman, US Patent No. 5, 622, 898.

Regarding claim 3, the combination of Uematsu and Yoshida does not disclose coaxial wire connecting the component and the coaxial via.

Zechman disclose such coaxial wire connecting the component and the substrate.

Further, such coaxial wire connection is used in the art to avoid the distortion of wire and resultant short circuit and to provide the shielding to the wire to avoid disturbances.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit package of the combination of Uematsu and Yoshida with the coaxial wire connection between the component and the substrate, as taught by Zechman, in order to have shielded coaxial wire connection.

Regarding claim 4, Yoshida further discloses each coaxial wire comprises a conductive bonding wire, a coating of insulating material and a conductive layer on the insulating material to form coaxial structure.

Regarding claim 13-15 and 31 and 32, the modified circuit assembly of Uematsu discloses all the features of the claimed inventions including the coaxial wire connection to the coaxial via as applied to claim 1-4 above.

Regarding claim 19-21, the modified circuit assembly of Uematsu discloses all the features of the claimed inventions including the electrically and thermally conductive base material and thermally matched to that of component as applied to claims 8, 9 and 10 above.

Regarding claim 22, the modified circuit assembly of Uematsu further discloses the conductive material on the wirer and the component, see Zechman figure 2.

6. Claims 5-7 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Uematsu, Yoshida and Zechman, as applied to claims 1-4 above, and further in view of Yamazaki et al., US Patent No. 6,191,492, Hereafter Yamazaki.

Regarding claims 5-7 and 16-18, the applicant is claiming a tapered transition at the coaxial wire connection.

Though the combination of Uematsu, Yoshida and Zechman does not explicitly disclose such transition, such transition is known in the art for apparent reason of getting better connections.

Further, Yamazaki disclose such transition on both the end of the wire; see Yamazaki figure 2A and 2B.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified circuit package of Uematsu with the transition and thicker insulation as taught by Yamazaki in order to have better and reliable electrical and mechanical connection.

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

(a) Argument: The new limitation "wherein each of the coaxial vias and the base form a substantially flat surface", not shown by prior art.

New prior art of Yoshida discloses the new limitation.

(b) Argument: No "coaxial connection" in applied prior art of Uematsu and further explains, " by definition, a ***coaxial connection*** includes two regions that electrically connect to one device to another. For example, the well-known coaxial cable consists of a tube of electrically conducting material surrounding a central conductor [The Merriam-Webster Dictionary, 50th Anniversary Edition, 1997].

Uematsu discloses the coaxial structure with central conductive material surrounded by the metallic base material, making a coaxial via, see Uematsu figure 1.

(c) Argument:

The "substantially flat" characteristic of the invention allows both the coaxial via and the base to be coated with a conductive layer (such as conductive layer 2 in Figure 2). The conductive layer is deposited on this flat surface such that it covers substantially all of the central contact area of the coaxial via and some of the insulating ring that surrounds the central contact area.

The new prior art discloses the "coaxial via" and " the substantially flat surface" and further detail as argued has not been explicitly claimed in the calms 1 and 2.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isatake Sawano discloses a through hole coaxial structure for matching characteristic impedance and improving high frequency characteristic.

Masayuki Sasaki, discloses coaxial line structure.

JP2001015654A discloses a coaxial structure reducing switching noise.

Yoneda Yoshihiro discloses a package with solder resist on the substrate body.

Otani et al., discloses semiconductor chip mounting board with solder resist 9.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (8:30 - 5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
August 5, 2003